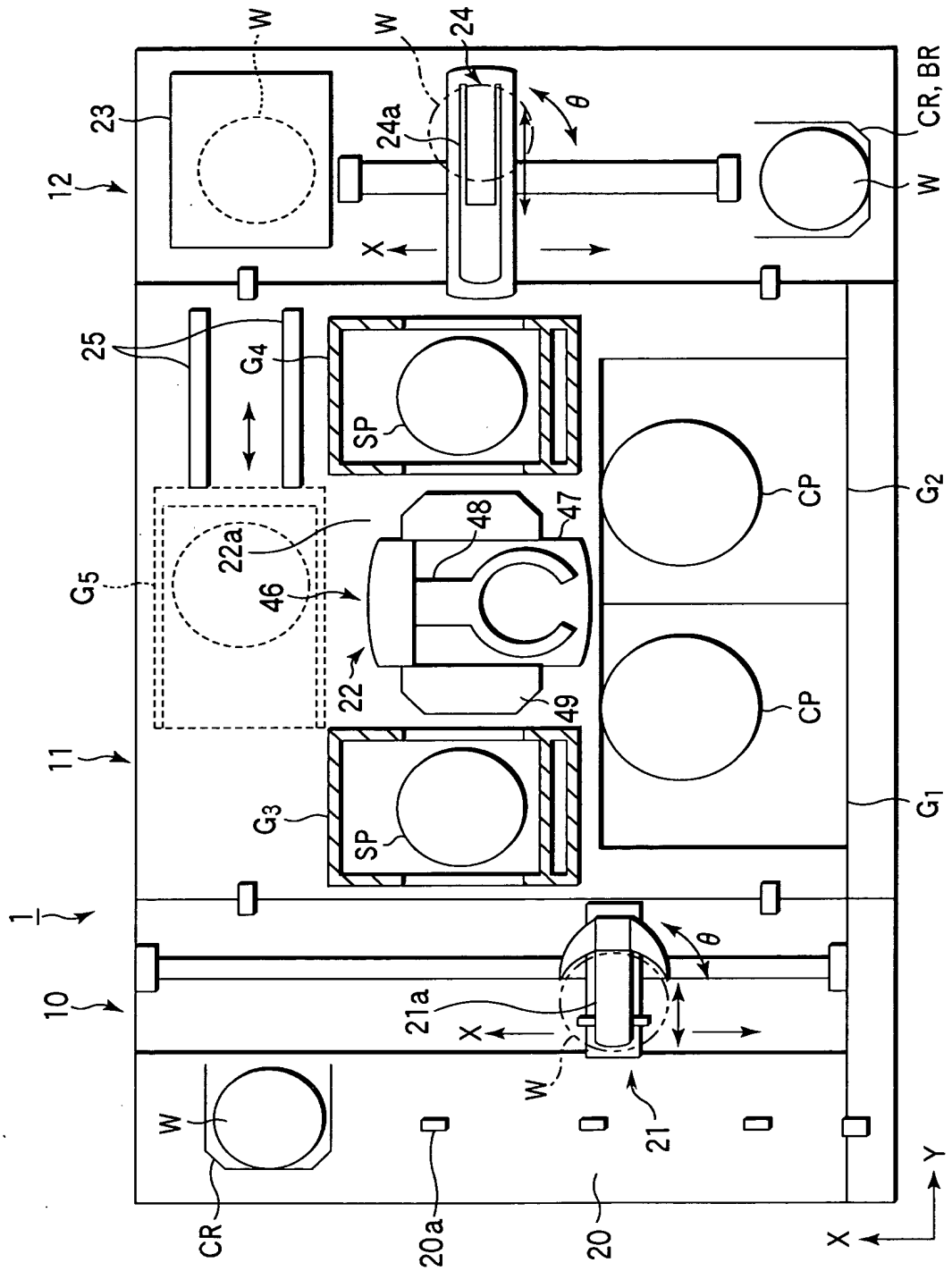
W
W
24
23
24a
θ
CR, BR
12
W
X
25
G4
SP
CP
G2
48
47
22a
G5
46
22
49
CP
11
G3
SP
G1
1
θ
10
21a
X
W
21
Y
W
CR
20a
20
X

FIG.1

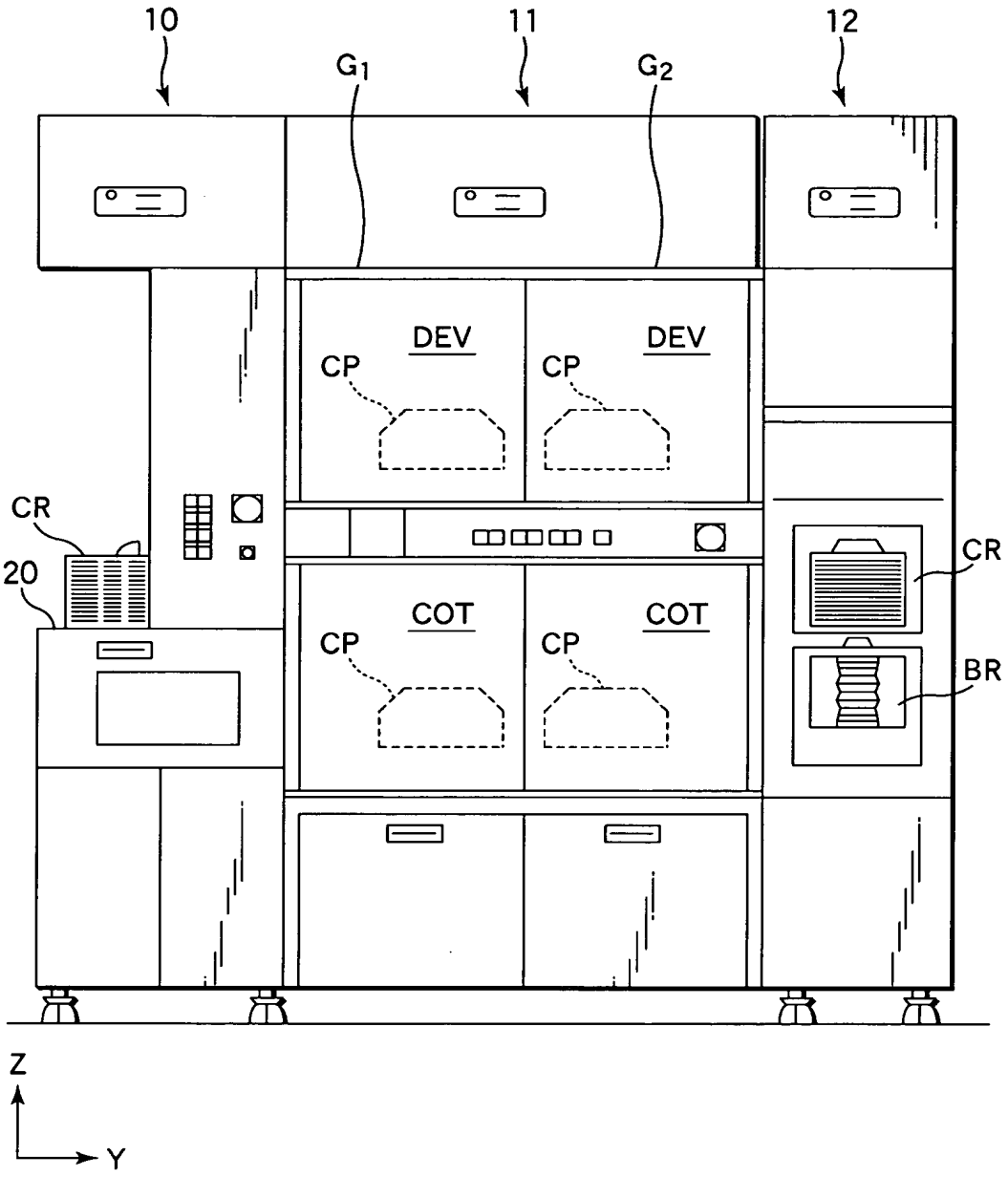

FIG.2

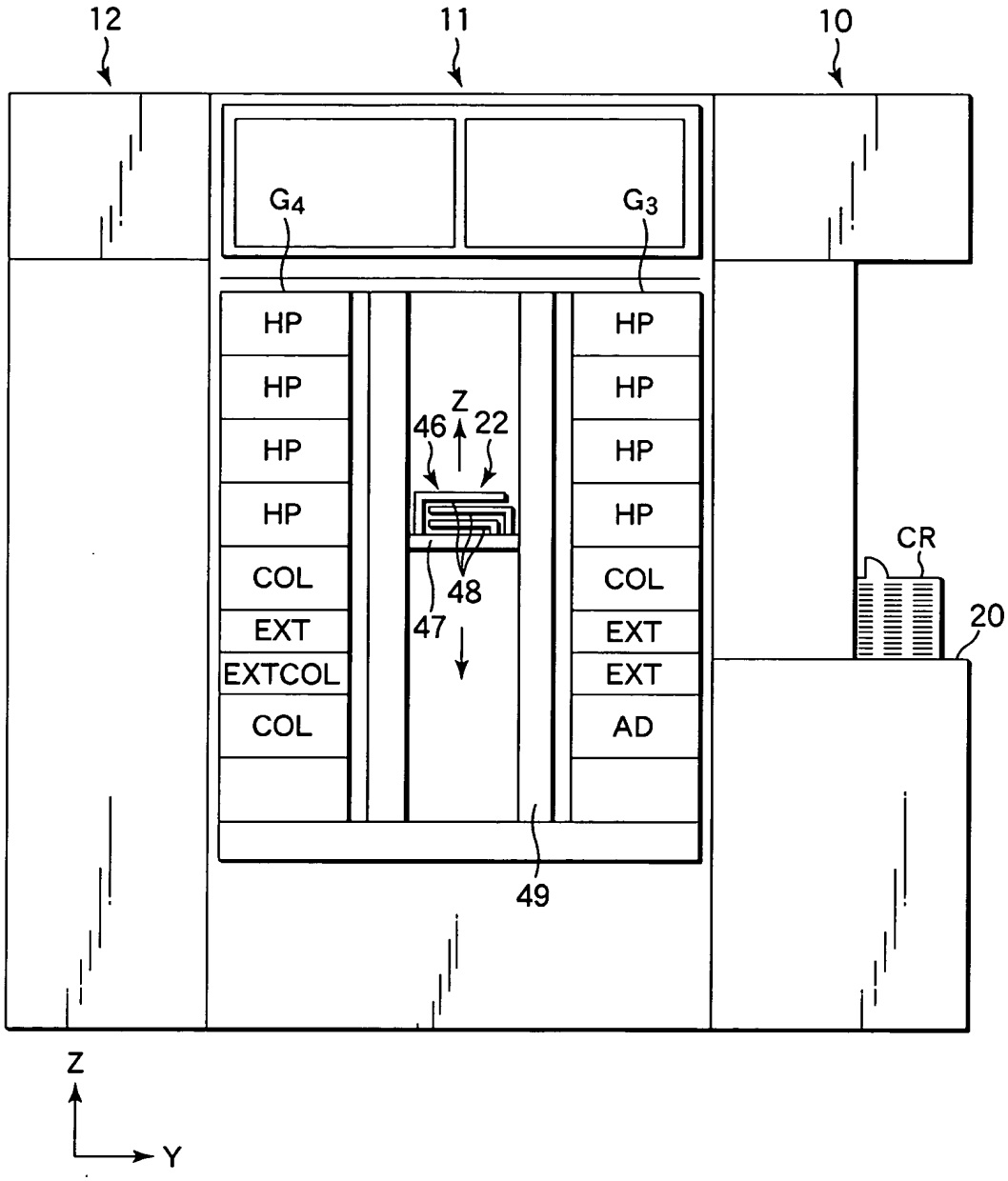
12
11
10
G4
G3
HP
HP
HP
HP
COL
EXT
EXTCOL
COL
HP
HP
HP
HP
COL
EXT
EXT
AD
Z
46
22
48
47
49
CR
20
Z
Y

FIG.3

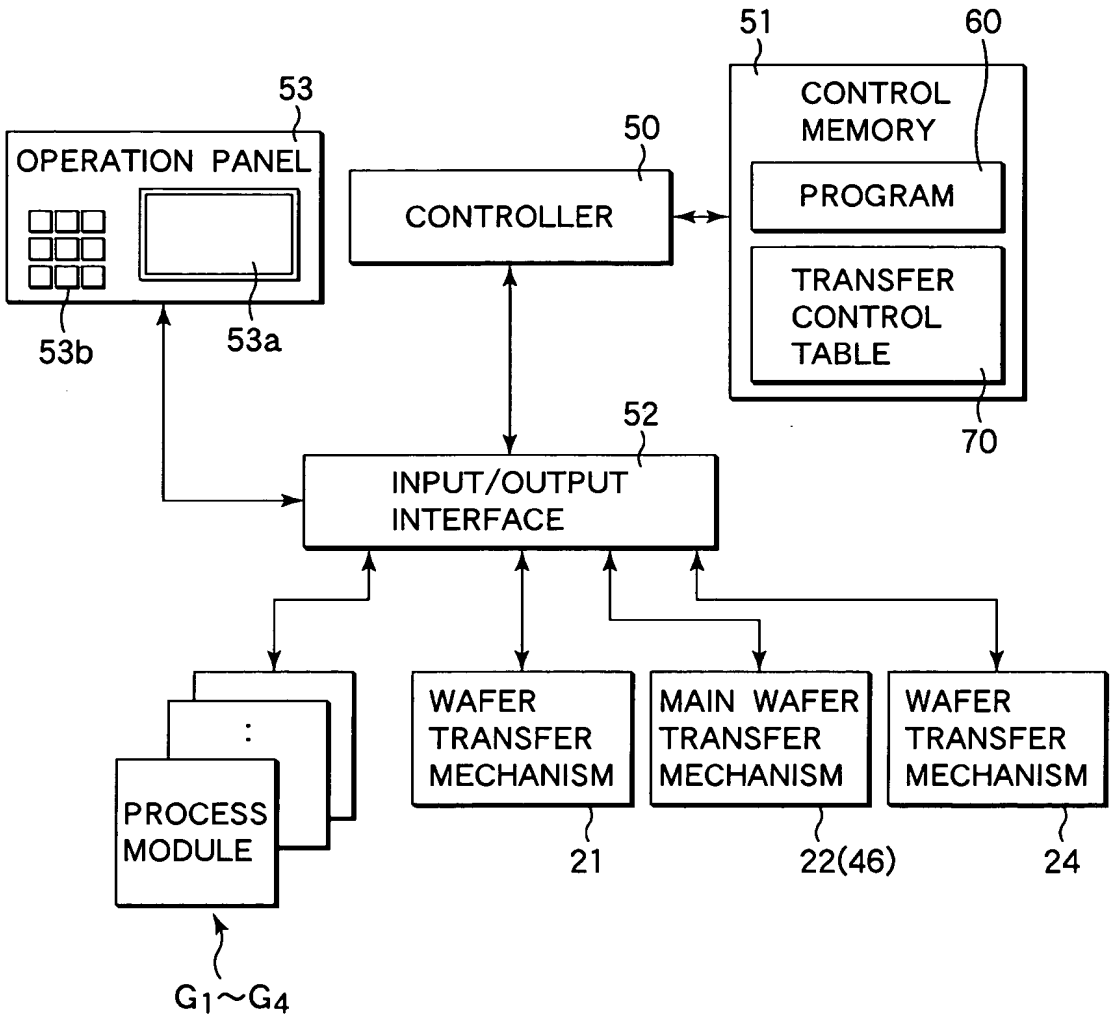
51
60
53
CONTROL MEMORY
50
OPERATION PANEL
CONTROLLER
PROGRAM
TRANSFER CONTROL TABLE
53b
53a
70
52
INPUT/OUTPUT INTERFACE
PROCESS MODULE
WAFER TRANSFER MECHANISM
MAIN WAFER TRANSFER MECHANISM
WAFER TRANSFER MECHANISM
21
22(46)
24
G1~G4

FIG.4

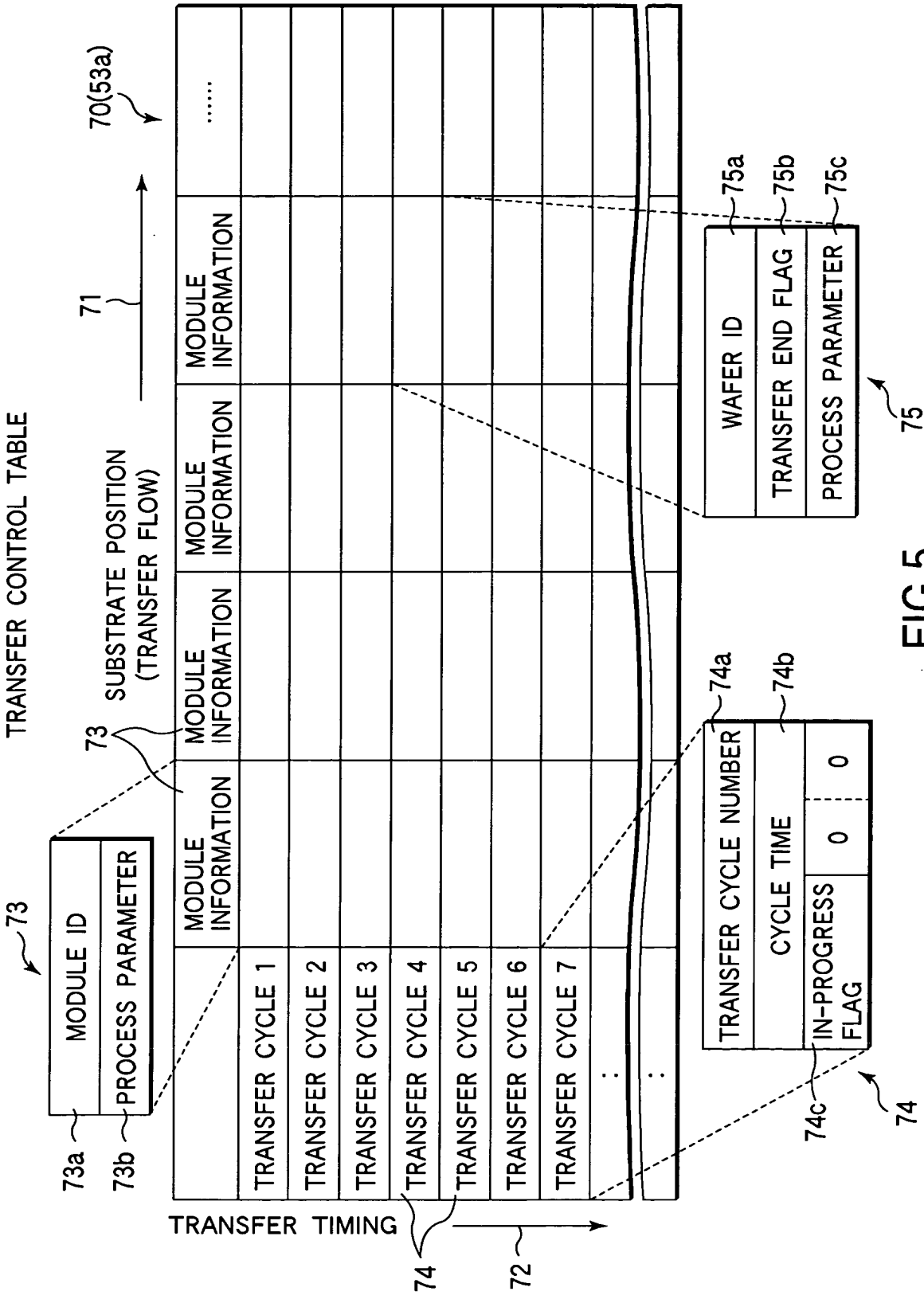
TRANSFER CONTROL TABLE
70(53a)
71
SUBSTRATE POSITION (TRANSFER FLOW)
73
MODULE INFORMATION
.....
TRANSFER CYCLE 1
TRANSFER CYCLE 2
TRANSFER CYCLE 3
TRANSFER CYCLE 4
TRANSFER CYCLE 5
TRANSFER CYCLE 6
TRANSFER CYCLE 7
TRANSFER TIMING
72
74
MODULE ID
PROCESS PARAMETER
73a
73b
WAFER ID
TRANSFER END FLAG
PROCESS PARAMETER
75a
75b
75c
75
TRANSFER CYCLE NUMBER
CYCLE TIME
IN-PROGRESS FLAG
0
0
74a
74b
74c

FIG.5

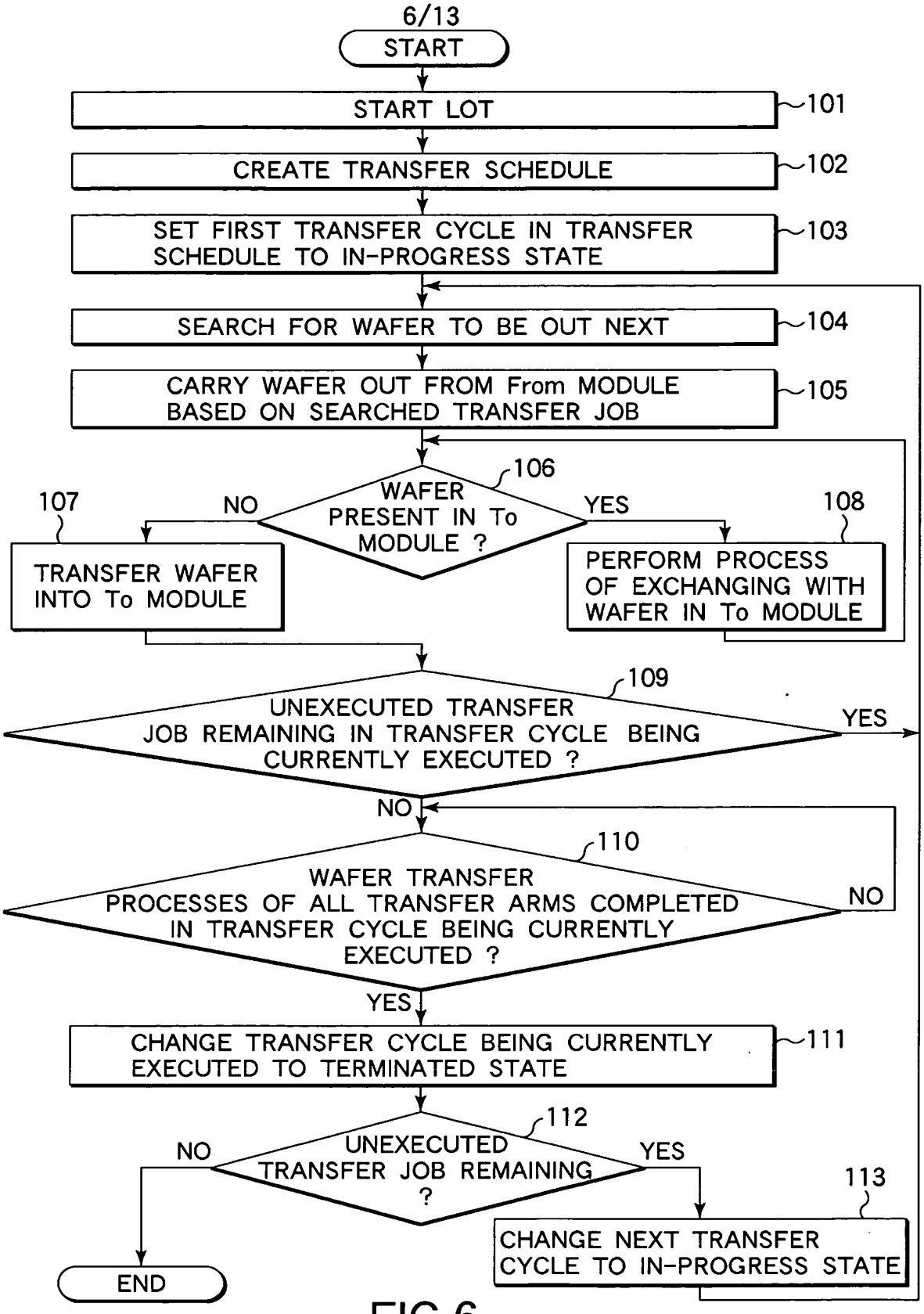
START
START LOT
101
CREATE TRANSFER SCHEDULE
102
SET FIRST TRANSFER CYCLE IN TRANSFER SCHEDULE TO IN-PROGRESS STATE
103
SEARCH FOR WAFER TO BE OUT NEXT
104
CARRY WAFER OUT FROM From MODULE BASED ON SEARCHED TRANSFER JOB
105
106
WAFER PRESENT IN To MODULE ?
NO
YES
107
TRANSFER WAFER INTO To MODULE
108
PERFORM PROCESS OF EXCHANGING WITH WAFER IN To MODULE
109
UNEXECUTED TRANSFER JOB REMAINING IN TRANSFER CYCLE BEING CURRENTLY EXECUTED ?
YES
NO
110
WAFER TRANSFER PROCESSES OF ALL TRANSFER ARMS COMPLETED IN TRANSFER CYCLE BEING CURRENTLY EXECUTED ?
NO
YES
CHANGE TRANSFER CYCLE BEING CURRENTLY EXECUTED TO TERMINATED STATE
111
112
UNEXECUTED TRANSFER JOB REMAINING ?
NO
YES
113
CHANGE NEXT TRANSFER CYCLE TO IN-PROGRESS STATE
END

FIG.6

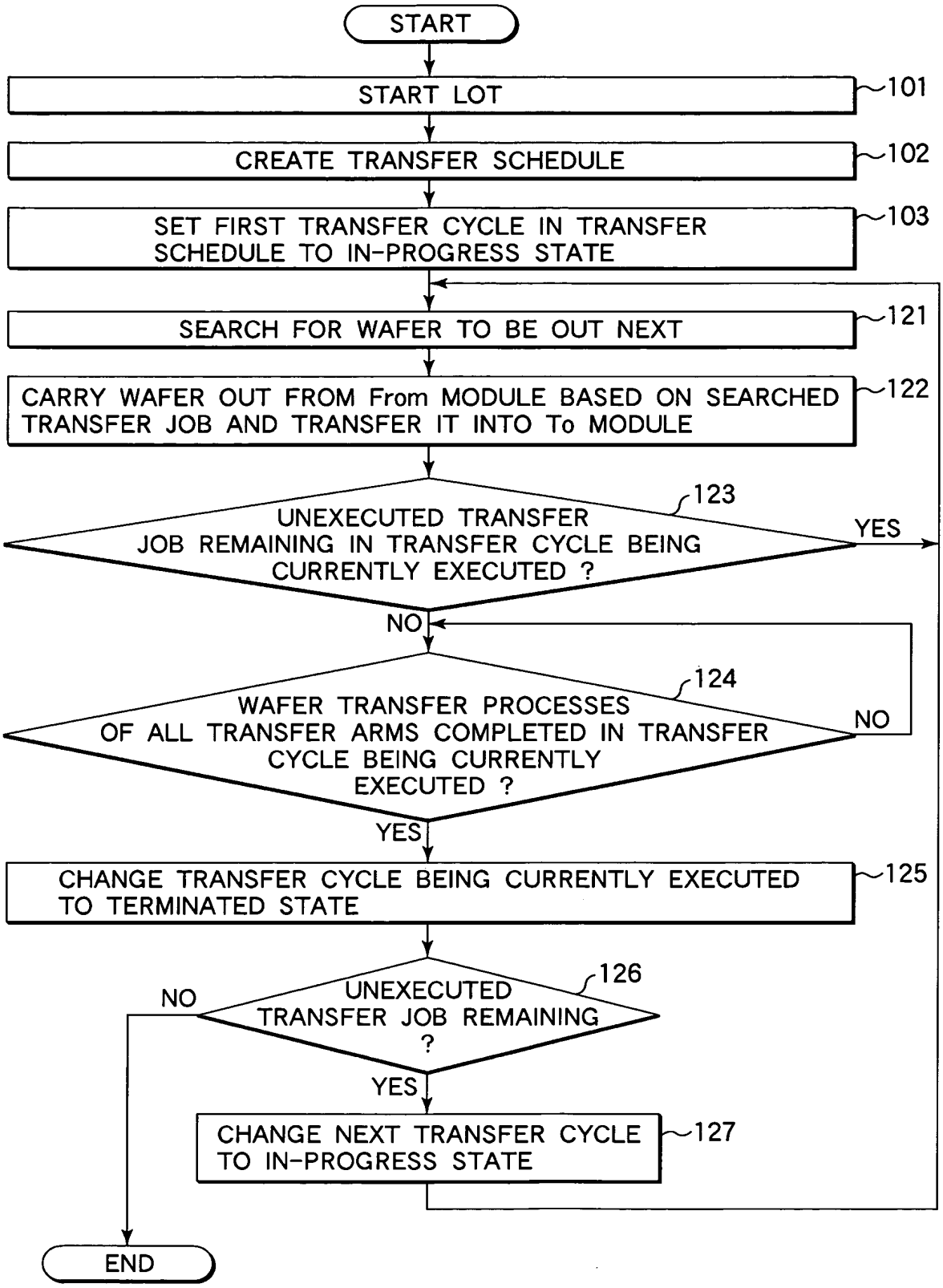
START
START LOT
101
CREATE TRANSFER SCHEDULE
102
SET FIRST TRANSFER CYCLE IN TRANSFER SCHEDULE TO IN-PROGRESS STATE
103
SEARCH FOR WAFER TO BE OUT NEXT
121
CARRY WAFER OUT FROM From MODULE BASED ON SEARCHED TRANSFER JOB AND TRANSFER IT INTO To MODULE
122
UNEXECUTED TRANSFER JOB REMAINING IN TRANSFER CYCLE BEING CURRENTLY EXECUTED ?
123
YES
NO
WAFER TRANSFER PROCESSES OF ALL TRANSFER ARMS COMPLETED IN TRANSFER CYCLE BEING CURRENTLY EXECUTED ?
124
NO
YES
CHANGE TRANSFER CYCLE BEING CURRENTLY EXECUTED TO TERMINATED STATE
125
UNEXECUTED TRANSFER JOB REMAINING ?
126
NO
YES
CHANGE NEXT TRANSFER CYCLE TO IN-PROGRESS STATE
127
END

FIG.7

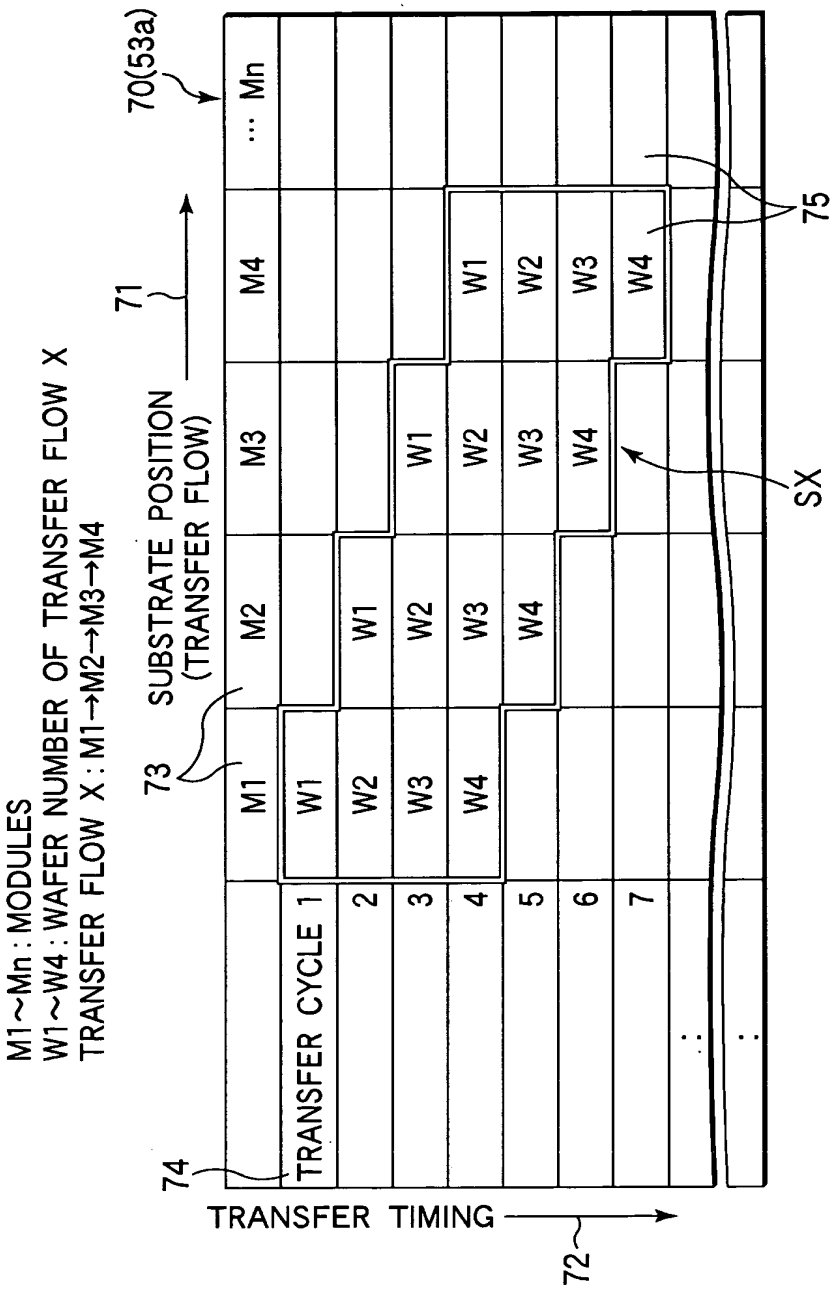
M1~Mn : MODULES
W1~W4 : WAFER NUMBER OF TRANSFER FLOW X
TRANSFER FLOW X : M1→M2→M3→M4
70(53a)
71
SUBSTRATE POSITION
(TRANSFER FLOW)
73
74
75
SX
M1
M2
M3
M4
... Mn
TRANSFER CYCLE 1
2
3
4
5
6
7
W1
W2
W3
W4
TRANSFER TIMING
72

FIG.8

M1～M6 : MODULES
A1～A5 : WAFER NUMBER OF LOT OF TRANSFER FLOW A
B1～B5 : WAFER NUMBER OF LOT OF TRANSFER FLOW B

TRANSFER FLOW A	M1→M2→M3→M4→M5→M6
TRANSFER FLOW B	M1→M2→M3→M5→M4→M6

FIG.9A

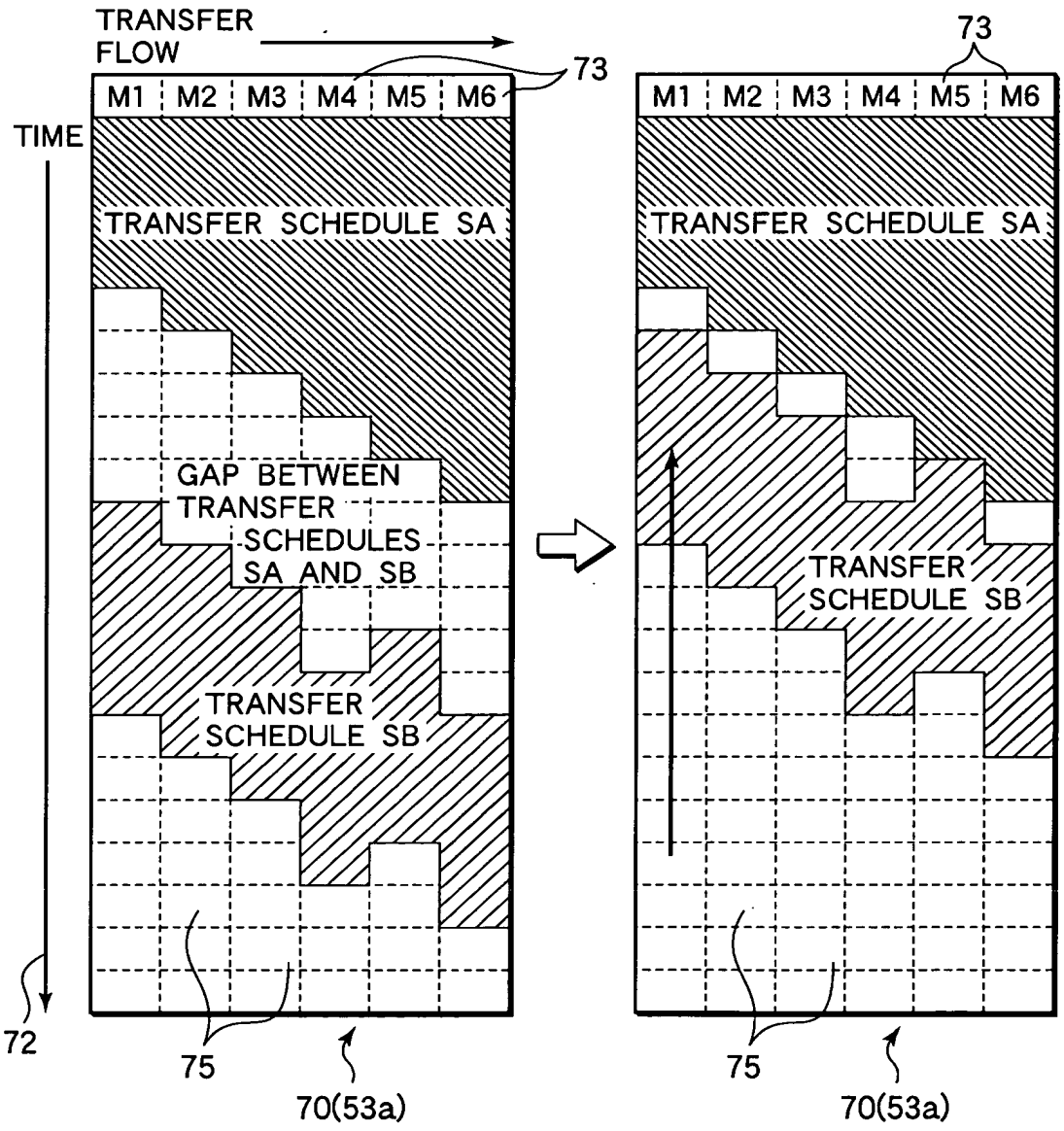

FIG.9B

FIG.9C

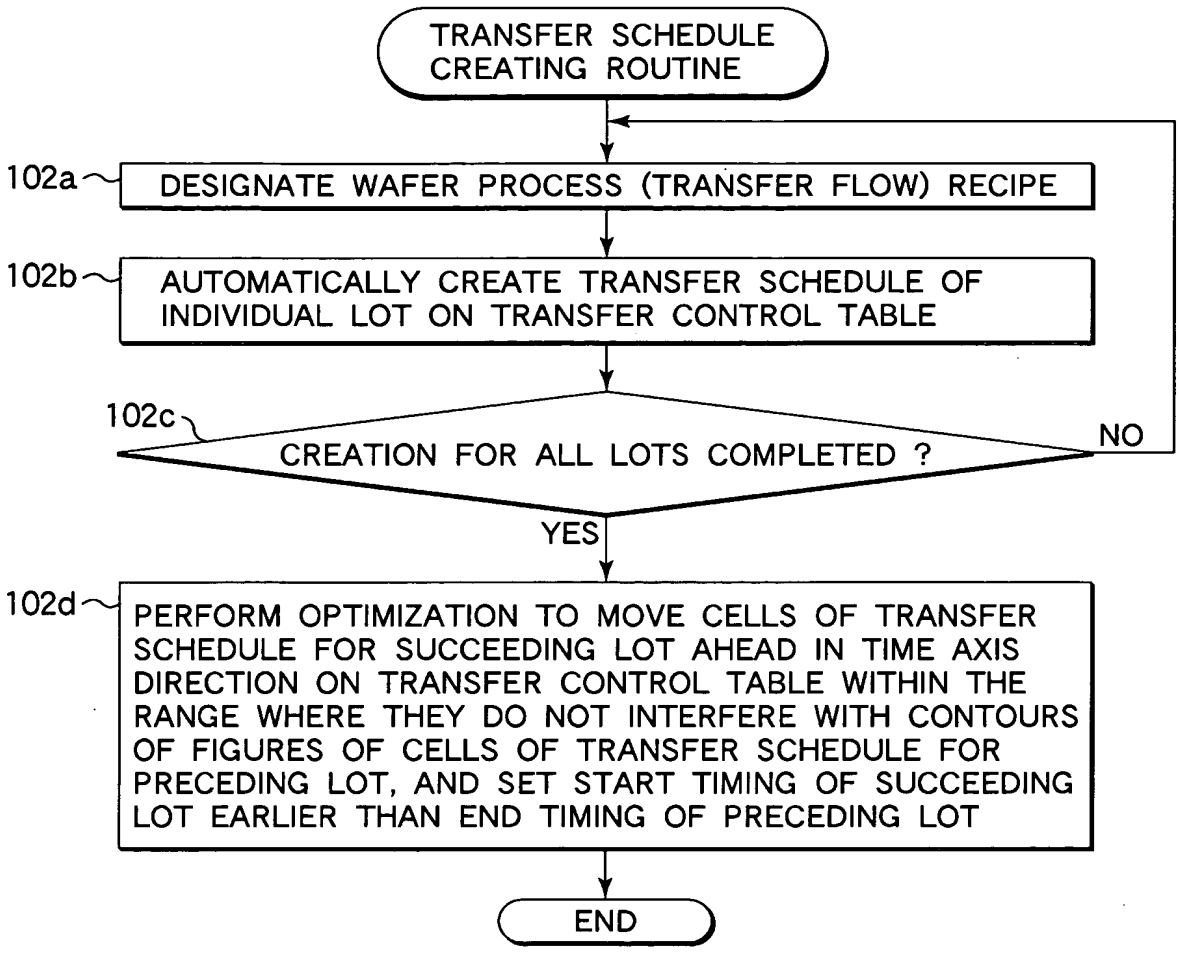
TRANSFER SCHEDULE CREATING ROUTINE
102a
DESIGNATE WAFER PROCESS (TRANSFER FLOW) RECIPE
102b
AUTOMATICALLY CREATE TRANSFER SCHEDULE OF INDIVIDUAL LOT ON TRANSFER CONTROL TABLE
102c
CREATION FOR ALL LOTS COMPLETED ?
NO
YES
102d
PERFORM OPTIMIZATION TO MOVE CELLS OF TRANSFER SCHEDULE FOR SUCCEEDING LOT AHEAD IN TIME AXIS DIRECTION ON TRANSFER CONTROL TABLE WITHIN THE RANGE WHERE THEY DO NOT INTERFERE WITH CONTOURS OF FIGURES OF CELLS OF TRANSFER SCHEDULE FOR PRECEDING LOT, AND SET START TIMING OF SUCCEEDING LOT EARLIER THAN END TIMING OF PRECEDING LOT
END

FIG.10

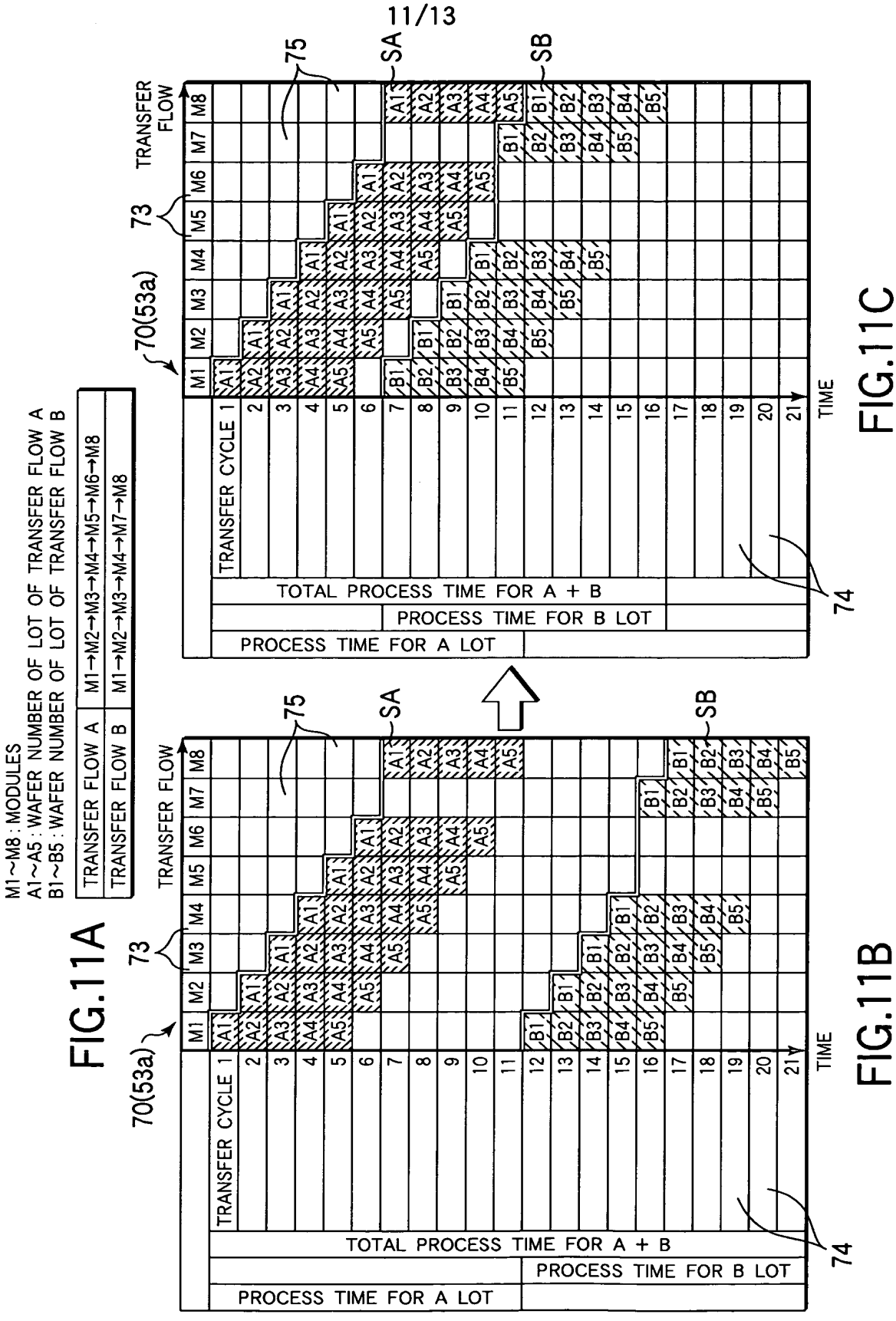

FIG.11A

FIG.11B

FIG.11C

M1~M6 : MODULES
EIS : EXPOSURE APPARATUS INTERFACE STAGE
BUF : BUFFER PRECEDING EXPOSURE APPARATUS (IN BUFFER)
A1~A5 : WAFER NUMBER OF LOT OF TRANSFER FLOW A
B1~B5 : WAFER NUMBER OF LOT OF TRANSFER FLOW B

TRANSFER FLOW A	M1→M2→M3→BUF→EIS→M4→M5→M6
TRANSFER FLOW B	M1→M2→M3→BUF→EIS→M4→M5→M6

FIG.12A

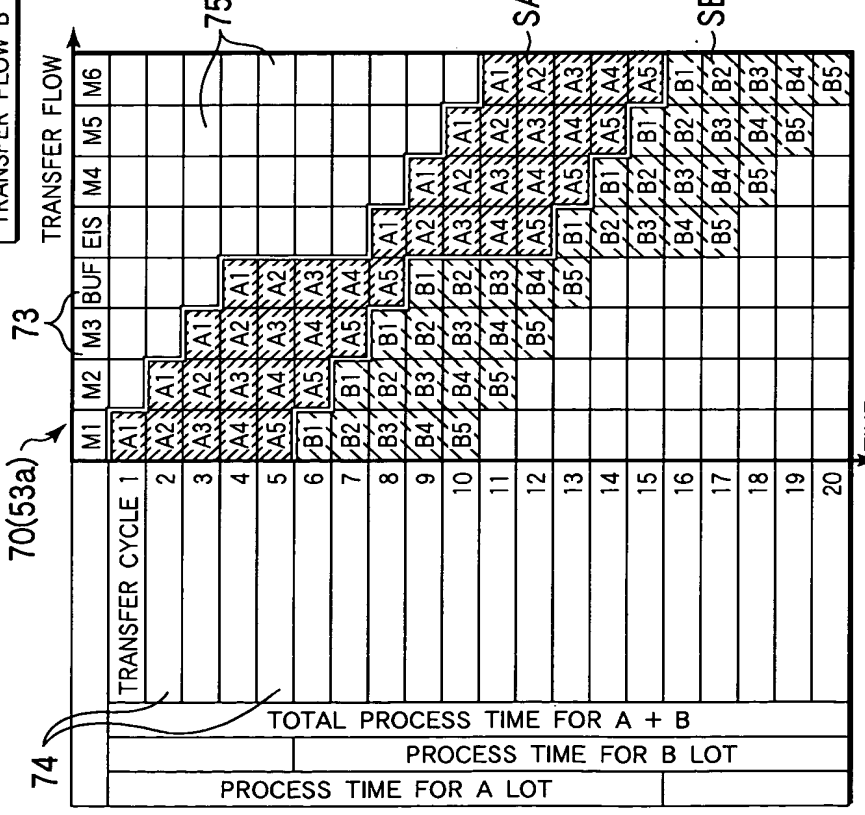

FIG.12B

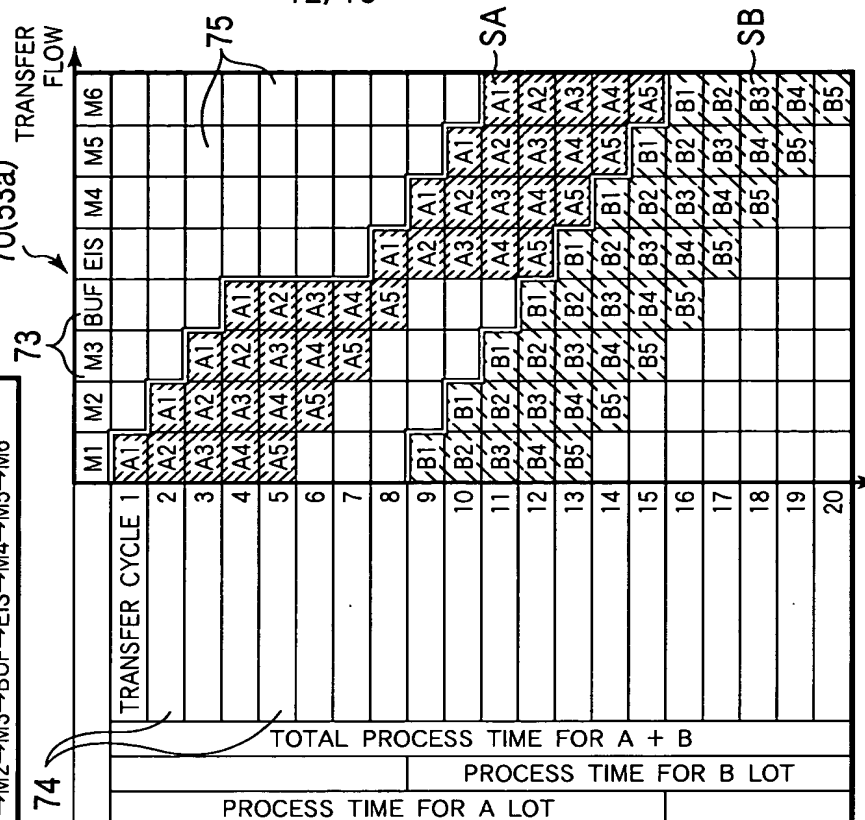

FIG.12C

M1～M8 : MODULES
A1～A5 : WAFER NUMBER OF LOT OF TRANSFER FLOW A
B1～B5 : WAFER NUMBER OF LOT OF TRANSFER FLOW B

TRANSFER FLOW A	M1→M2→M3→M4→M6→M7→M8 M5
TRANSFER FLOW B	M1→M2→M3→M4→M5→M6→M7→M8

FIG.13A

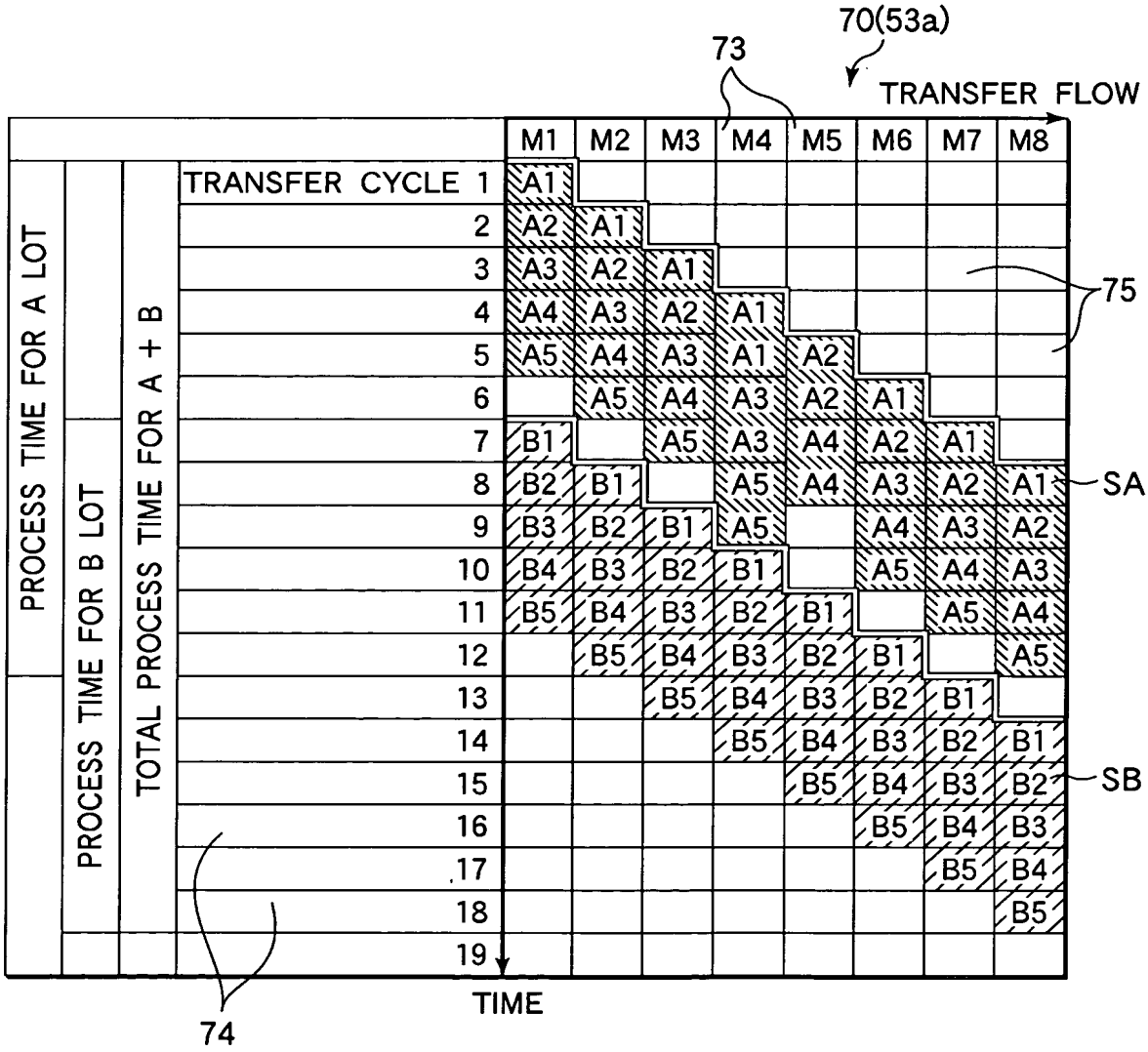

FIG.13B